REMARKS

I. Rejections Under 35 U.S.C. § 103(a)

In the Office Action dated January 5, 2004, claims 29-39 were rejected by the Examiner in Paper No. 9 under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art (APA) in view of U.S. Patent No. 6,417,088 to Ho et al ("Ho").

Regarding claim 29, the Examiner argued that APA discloses a method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit (IC) device in fig. 2 comprising the steps of: providing a substrate, thereafter configuring substrate to comprise a wiring bond pad to comprise a single metal layer 42, fig. 2, wherein the single metal layer does not share a single metal layer with any other material, thereafter positioning at least one IC device below, specification 3 [006] [007] wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer, thereafter locating the single metal layer 28 above a plurality of intermetal dielectric (IMD) layers 46, fig. 2, specification page 9 [0027] and thereafter locating at least one IC device below the plurality of IMD layers, wherein the single metal layer comprises a metal-8 layer 28.

The Applicants respectfully disagree with this assessment. Layer 42, Fig. 2 of the APA does not show the step of configuring a substrate to comprise a wiring bond pad to comprise a single metal layer, wherein the single metal layer does not share a single metal layer with any other material. Instead, Fig. 2 shows a bond pad 24 composed of a number of layers 28, 30, 32, 34, 36, 38, 40 and 42. The bond pad 24 of Fig. 2 is thus NOT formed from a single metal layer, but IS formed from a number of 28, 30, 32, 34, 36, 38, 40 and 42.

FIG. 2 of Applicants' specification depicts a block diagram of a prior art conventional wiring bond pad 24. Bond pad 24 is indicated in FIG. 2 to illustrate the

fact that traditional wiring bond pads are generally full layer structures. For example, in FIG. 2, metal-1 (M1) to metal-8 (M1) layers are indicated. An M1 layer 42 thus is positioned below an M2 layer 40, while an M3 layer 38 is located below an M4 layer 36. An M5 layer 34 is positioned below an M6 layer 32, while an M7 layer 30 is positioned below an M8 layer 28. Traditional wiring bond pad design rules generally do not permit *only one* metal layer to be utilized for implementing a wiring bond pad due to wiring bond stress-induced fracture during packaging. Bonding mechanical stresses are indicated in FIG. 2 by arrow 26, which also illustrates the general direction of such bonding mechanical stresses.

Additionally IMD1 to IMD 7 layers are illustrated, as indicated by arrows 46. An interlayer dielectric (ILD) is indicated by arrow 44. Via-1 to Via 7 are also depicted in FIG. 2. It is thus apparent that a major difference between the configurations of FIG. 1 and FIG. 2 lies in the ability of the design illustrated in FIG. 1 to form a wiring bond pad from a single metal layer, without experiencing stress-induced fractures. The design depicted in FIG. 2 will suffer from stress-induced fractures, if an attempt is made to implement a single metal layer as a wiring bond pad. Thus, it is clear that the APA does NOT teach, disclose or suggest a wiring bond pad comprised of a single metal layer.

The Examiner further argued that the specification at page 3, paragraphs [006] [007], teaches the step of thereafter positioning at least one IC device below, a wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer. The Applicants respectfully disagree with this conclusion. Paragraphs [006] [007] do NOT teach a wiring bond pad formed from a single metal layer. Additionally, paragraphs [006] [007] does not teach positioning at least one IC device below, a wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer.

Instead paragraph [006] teaches that after an integrated circuit is fabricated, external connections must be formed before the chip is embedded in plastic for protection. With aluminum wiring, which has been the standard for many years, the upper level of wiring for the chip would include bond pads with necessary connections to the underlying circuit. After the protective overcoat (PO) layer is deposited over the chip, holes are etched through the PO to provide access to the bond pads. Depending on the type of packaging used, external connections from the chip can then be made by thin wires which are typically ultrasonically bonded to the bond pad, or by the formation of solder balls which make a direct connection between the bond pad on the chip and the external connector.

Paragraph [007] teaches that traditional wiring bonds pads have been configured as full layer structures. For example, traditional wiring bonds pads have been arranged as metal-1 to metal-8 structures in an eight-layer metal process. Current wiring pad design rules do not permit only one layer for wiring bond configurations, due to wire bonding stress-reduced fractures that can result during packaging. Devices present under wiring pads have also been prohibited according to traditional wiring bond pad rules. It is clear from the foregoing that neither paragraph [007] or [006] make any mention of the step of thereafter positioning at least one IC device below the wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer. The Examiner has not properly explained why this is so.

The Examiner additionally argued that Fig. 2, teaches thereafter locating the single metal layer 28 above a plurality of intermetal dielectric (IMD) layers 46, fig. 2, specification page 9 [0027] and thereafter locating at least one IC device below the plurality of IMD layers, wherein the single metal layer comprises a metal-8 layer 28. Applicants respectfully disagree with this assessment. Fig. 2 does NOT teach a wiring bond pad formed from a single metal layer located above a plurality of IM

layers. Instead, Fig. 2 and page 9, paragraph [0027] depict merely a wiring bond pad 24 formed from a plurality of layers 28, 30, 32, 34, 36, 38, 40 and 42. Such layers are respectively located between IMD layers 46. This is a far cry from a wiring bond pad formed from a single metal layer located above a plurality of IMD layers. Thus, layer 28 is one of many layers that form a wiring bond bad, while Applicants' claim, on the other hand, a wiring bond bad comprising a single metal layer, not a plurality of layers.

The Applicants invite the Examiner to review Applicants' Fig. 1, which clearly shows a wiring bond pad from a single metal layer 12 rather than a bond bad formed from a plurality of layers, such as layers 28, 30, 32, 34, 36, 38, 40 and 42. Regarding the fact that Applicants' refer to a metal-8 layer for forming the single metal layer (which forms the wiring bond pad), Applicants' submit that the Examiners mention of thereafter locating at least one IC device below the plurality of IMD layers, wherein the single metal layer comprises a metal-8 layer 28 is irrelevant in light of the fact that the APA, as indicated above, does not teach, disclose or suggest a wiring bond pad formed from a single metal later. Instead, the APA teaches a wiring bond pad formed from a number of metal layers rather than only a single metal layer. Applicants point out that the word "single" is significant because it means "one" rather than a plurality of layers.

The Examiner admitted that APA does not expressly disclose locating a buffer and bonding layer immediately above a single metal layer 28. The Examiner argued, however, that Ho discloses a method for forming a wiring bond pad 30, column, 3, line 10, comprising an aluminum buffer layer 52, Fig. 6, column 4, lines 1 and bonding layer 60, column 4, line 53, immediately above single metal layer 30. The Examiner argued that at the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the buffer layer and bonding layer teaching of Ho with APA, because it would have increased the adhesion

between the bond pad and the bonding layer as taught by Ho, column, 4, lines 30-32.

The Applicants respectfully disagree with this assessment. Ho shows separate bonding and buffer layers not a layer that functions as both as bonding and buffer layer. Thus, it is improper to suggest that Ho shows both a layer that functions as both a buffer and bonding layer. In fact, because the buffer and bonding layers of Ho are separate layers, Ho teaches away from the use of a combined buffer and bonding layer. Thus, Ho can not properly be combined with the APA to teach a layer that functions as both a buffer and bonding layer.

Additionally, Ho does not teach or suggest a wiring bond pad comprising only a single metal layer, wherein the single metal layer does not share the single metal layer with any other material. Applicants refer the Examiner to a copy of FIG. 6 of Ho below, and a mark-up thereof, which indicates that FIG. 6 shows at least two different types of materials located on the same single layer. Additionally, neither Ho nor APA teach a single layer composed only of a metal-8 layer. Thus, because neither Ho nor the APA teach a wiring bond pad comprising a single metal layer, wherein the single metal layer does not share the single metal layer with any other material, Ho and APA cannot properly be combined within one another as a basis for rejection claim 29 under 35 U.S.C. 103 (a). The Applicants therefore submit that the rejection to claim 29 under 35 U.S.C. 103 (a) has been traversed. Applicants therefore request withdrawal of the rejection to claim 29 under 35 U.S.C. 103 (a).

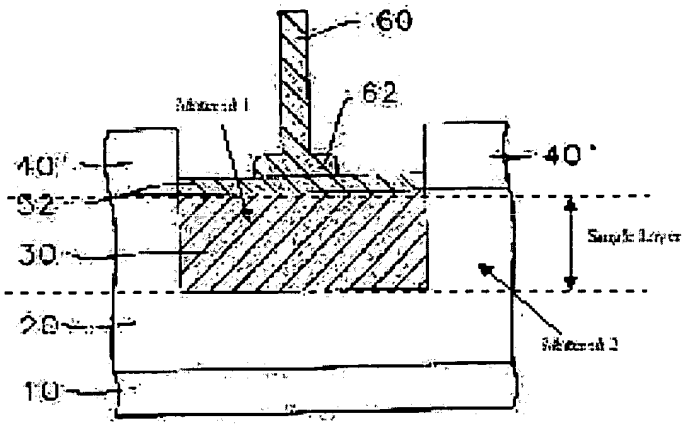

FIG. 6

Regarding claim 30, the Examiner argued that the APA discloses a method wherein the plurality of IMD layers comprises at least IMD-1 to IMD-7 layers 46, fig. 2, specification page 9 [0027]. The Applicants respectfully disagree with this assessment. Applicants' claim 30, which depends from claim 29, teaches that the plurality of intermetal dielectric layers comprises at least IMD-1 to IMD-7 layers. Applicants' claim 29, from which claim 30 depends, teaches that the single metal layer is formed above a plurality of intermetal dielectric layers. Recall that the single metal layer makes up the wiring bond pad. The wiring bond pad of Applicants' invention, as indicated above, is formed from a single metal layer, NOT a plurality of layers.

Layers 46 shown in Fig. 2 are disposed between a plurality of layers 28, 30, 32, 34, 36, 38, 40 and 42 which make up a wiring bond pad 24. Thus, it is clear that the APA at Fig. 2, layers 46 and the specification at page 9, paragraph [0027] do NOT teach a plurality of IMD layers formed below a single metal layer that makes up wiring bond pad. Rather, the APA at Fig. 2, layers 46 and the specification at page 9, paragraph [0027] teaches a plurality of layers 46 disposed between a plurality of metal layers that form a wiring bond pad. Thus, the

Applicants submit that the rejection to claim 30 has been traversed. Applicants therefore request that the rejection to claim 30 under 35 U.S.C. 103 (a) be withdrawn.

Regarding claim 31, the Examiner admitted that the APA does not expressly disclose the metal-8 layers 28 comprising a copper layer. The Examiner argued, however, that Ho discloses a bond pad 30 comprising copper, column 3, line 36. The Examiner therefore argued that at the time the invention was made, it would have been obvious to one of ordinary skill in the art to use the copper bonding pad teach of Ho with APA, because such copper material is conventional and would have been considered a mere substitution of art-recognized equivalent values. The Applicants respectfully disagree with this assessment.

The Applicants submit that all of the arguments presented above with respect to the rejection to claims 29 and 30 apply equally to the rejection to claim 31. Thus, Ho cannot properly be combined with APA as a basis for rejecting claim 31, because Ho does not teach or suggest a wiring bond pad comprising only a single metal layer, wherein the single metal layer does not share the single metal layer with any other material. Additionally, neither Ho nor APA teach a single layer composed only of a metal-8 layer formed from copper. Thus, because neither Ho nor the APA teach a wiring bond pad comprising a single metal layer, wherein the single metal layer does not share the single metal layer with any other material, Ho and APA cannot properly be combined within one another as a basis for rejecting claim 21 under 35 U.S.C. 103 (a). The Applicants therefore submit that the rejection to claim 31 under 35 U.S.C. 103 (a) has been traversed. Applicants therefore request withdrawal of the rejection to claim 31 under 35 U.S.C. 103 (a).

Regarding claim 32, the Examiner argued that the APA discloses a method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit (IC) device comprising the steps of: providing a substrate, thereafter

configuring the substrate to comprise a wiring bond pad to comprise a single metal layer 42, Fig. 2, wherein the single metal layer does not share a single metal layer with any other material, thereafter locating at least one IC device below the wiring bond pad, specification page 3 [006]-[007], to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer, 28/30/32/34/36/38/40/42, fig. 2, thereafter locating a single metal layer above a plurality of IMD layers 46, wherein a plurality of IMD layers comprises at least IMD-1 to IMD-7, fig. 2, and thereafter locating at least one IC device below the plurality of IMD layers, wherein the single metal layer comprises a metal-8 -28.

The Examiner admitted that the APA does not expressly disclose locating a buffer and bonding layer immediately above the single metal layer comprises a layer having a thickness in a range of and including 10KÅ to 20KÅ. The Examiner argued, however, that Ho discloses the method for forming a wiring bond pad 30, column 3, lines 10, comprising an aluminum buffer layer 52, Fig. 6, column 4, line 1, and a bonding layer 60, column 4, line 53, immediately above single metal layer 30. The Examiner stated that at the time the invention was made, it would have been obvious to one of ordinary skill in the art to combine the buffer layer and bonding layer teaching of Ho with APA, because it would have increased the adhesion between the bond pad and the bonding layer as taught by Ho, column 4, lines 30-32.

The Applicants respectfully disagree with this assessment. Ho shows separate bonding and buffer layers, which were identified by the Examiner, rather a layer that functions as both as bonding and buffer layer. Thus, it is improper to suggest that Ho teaches a layer that functions as both a buffer and bonding layer. In fact, because the buffer and bonding layers of Ho are separate layers, Ho teaches away from the use of a combined buffer and bonding layer. Thus, Ho can

not properly be combined with the APA to teach a layer that functions as both a buffer and bonding layer.

The Applicants further submit that the arguments presented above with respect to the rejections to claims 29-31 also apply to the rejection to claim 32. The Examiner argued that the group of layers 28, 30, 32, 34, 36, 38, 40 and 42 show a single metal layer. The Examiner is incurred because layers 28, 30, 32, 34, 36, 38, 40 and 42 represent a group of layers 28, 30, 32, 34, 36, 38, 40 and 42 that make up a wiring bond pad, while Applicants' claim 32 teaches a wiring bond pad formed from a single metal layer, NOT multiple layers 28, 30, 32, 34, 36, 38, 40 and 42. This is the reason the Applicants use the term "single" because this refers to "one" not a group of layers.

Layer 42, Fig. 2 of the APA does not show the step of configuring a substrate to comprise a wiring bond pad to comprise a single metal layer, wherein the single metal layer does not share a single metal layer with any other material. Instead, Fig. 2 shows a bond pad 24 composed of a number of layers 28, 30, 32, 34, 36, 38, 40 and 42. Layer 42 is one of a number of layers rather than a single layer. The bond pad 24 of Fig. 2 is thus NOT formed from a single metal layer, but IS formed from a number of layers 28, 30, 32, 34, 36, 38, 40 and 42.

APA FIG. 2 depicts a block diagram of a prior art conventional wiring bond pad 24. Bond pad 24 is indicated in FIG. 2 to illustrate the fact that traditional wiring bond pads are generally full layer structures. For example, in FIG. 2, metal-1 (M1) to metal-8 (M1) layers are indicated. An M1 layer 42 thus is positioned below an M2 layer 40, while an M3 layer 38 is located below an M4 layer 36. An M5 layer 34 is positioned below an M6 layer 32, while an M7 layer 30 is positioned below an M8 layer 28. Traditional wiring bond pad design rules generally do not permit *only one* metal layer to be utilized for implementing a wiring bond pad due to wiring bond stress-induced fracture during packaging. Bonding mechanical stresses are

indicated in FIG. 2 by arrow 26, which also illustrates the general direction of such bonding mechanical stresses.

Additionally IMD1 to IMD 7 layers are illustrated, as indicated by arrows 46. An interlayer dielectric (ILD) is indicated by arrow 44. Via-1 to Via 7 are also depicted in FIG. 2. It is thus apparent that a major difference between the configurations of FIG. 1 and FIG. 2 lies in the ability of the design illustrated in FIG. 1 to form a wiring bond pad from a single metal layer, without experiencing stress-induced fractures. The design depicted in FIG. 2 will suffer from stress-induced fractures, if an attempt is made to implement a single metal layer as a wiring bond pad. Applicants' claims, on the other hand, teach a method for forming a wiring bond pad composed of a single layer only, which prevents wiring bond stress-induced factures. The wiring bond pad 24, on the other hand is subject to such fractures because of the presence of multiple metal layers 28, 30, 32, 34, 36, 38, and 40, rather than simply a single metal layer. Thus, it is clear that the APA does NOT teach, disclose or suggest a wiring bond pad comprised of a single metal layer.

The Examiner further argued that the specification at page 3, paragraphs [006] [007], teaches the step of thereafter positioning at least one IC device below, a wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer. The Applicants respectfully disagree with this conclusion. Paragraphs [006] [007] do NOT teach a wiring bond pad formed from a single metal layer. Additionally, paragraphs [006] [007] does not teach positioning at least one IC device below, a wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer.

Instead paragraph [006] teaches that after an integrated circuit is fabricated, external connections must be formed before the chip is embedded in plastic for

protection. With aluminum wiring, which has been the standard for many years, the upper level of wiring for the chip would include bond pads with necessary connections to the underlying circuit. After the protective overcoat (PO) layer is deposited over the chip, holes are etched through the PO to provide access to the bond pads. Depending on the type of packaging used, external connections from the chip can then be made by thin wires which are typically ultrasonically bonded to the bond pad, or by the formation of solder balls which make a direct connection between the bond pad on the chip and the external connector.

Paragraph [007] teaches that traditional wiring bonds pads have been configured as full layer structures. For example, traditional wiring bonds pads have been arranged as metal-1 to metal-8 structures in an eight-layer metal process. Current wiring pad design rules do not permit only one layer for wiring bond configurations, due to wire bonding stress-reduced fractures that can result during packaging. Devices present under wiring pads have also been prohibited according to traditional wiring bond pad rules. It is clear from the foregoing that neither paragraph [007] or [006] make any mention of the step of thereafter positioning at least one IC device below the wiring bond pad to thereby conserve IC space and improve wiring bond pad efficiency as a result of configuring the wiring bond pad to comprise a single metal layer. The Examiner has not properly explained why this is so.

The Examiner additionally argued that Fig. 2, teaches thereafter locating the single metal layer 28 above a plurality of intermetal dielectric (IMD) layers 46, fig. 2, specification page 9 [0027] and thereafter locating at least one IC device below the plurality of IMD layers, wherein the single metal layer comprises a metal-8 layer 28. Applicants respectfully disagree with this assessment. Fig. 2 does NOT teach a wiring bond pad formed from a single metal layer located above a plurality of IM layers. Instead, Fig. 2 and page 9, paragraph [0027] depict merely a wiring bond pad 24 formed from a plurality of layers 28, 30, 32, 34, 36, 38, 40 and 42. Such

layers are respectively located between IMD layers 46. This is a far cry from a wiring bond pad formed from a single metal layer located above a plurality of IMD layers. Thus, layer 28 is one of many layers that form a wiring bond bad, while Applicants' claim, on the other hand, a wiring bond bad comprising a single metal layer, not a plurality of layers.

The Applicants invite the Examiner to review Applicants' Fig. 1, which clearly shows a wiring bond pad from a single metal layer 12 rather than a bond bad formed from a plurality of layers, such as layers 28, 30, 32, 34, 36, 38, 40 and 42. Regarding the fact that Applicants' refer to a metal-8 layer for forming the single metal layer (which forms the wiring bond pad), Applicants' submit that the Examiners mention of thereafter locating at least one IC device below the plurality of IMD layers, wherein the single metal layer comprises a metal-8 layer 28 is irrelevant in light of the fact that the APA, as indicated above, does not teach, disclose or suggest a wiring bond pad formed from a single metal later. Instead, the APA teaches a wiring bond pad formed from a number of metal layers rather than only a single metal layer. Applicants point out that the word "single" is significant because it means "one" rather than a plurality of layers, which the APA does show, but which is not taught by Applicants' claims. Based on the foregoing, the Applicants therefore submit that the rejection to claim 32 under 35 U.S.C. 103 (a) has been traversed. Applicants therefore request withdrawal of the rejection to claim 32 under 35 U.S.C. 103 (a).

Regarding claims 33-37, the Examiner admitted that the APA does not disclose the aluminum film formed from above single metal layer having a thickness in a range of 10KA-20KA, and wherein the single metal layer comprises a copper layer having a thickness of approximately 10-18KA. The Examiner argued, however, that the Ho reference discloses a method for forming a copper wiring pond pad 30, fig. 6, comprising an aluminum buffer layer 52, column 3, line 3, and bonding layer 60, column 4, line 53, immediately above metal layer 30, wherein the

aluminum buffer layer has a thickness in range of 5000Å, column 4, line 35. The Examiner therefore argued that it would have been obvious to one of ordinary skill in the art to use the buffer layer 52 teaching of Ho in the range as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover optimum or workable range by routine experimentation.

The Applicants respectfully disagree with this assessment. As indicated above, layers 28, 30, 32, 34, 36, 38, 40 and 42 do NOT form a single metal layer. The Examiner referred to single metal layer 42/40/38/36/34/32/30/28. The Examiner is incorrect in referring to multiple layers 42/40/38/36/34/32/30/28 as being a single metal later. Rather multiple layers 28, 30, 32, 34, 36, 38, 40 and 42 are multiple layers, which form a wiring bond pad 24. Applicants teach via claims 33-37, including claims from which claims 33-37 depend, a wiring bond pad formed from a single metal layer, wherein the single metal layer comprises a layer comprised of only one type of metal and does not share the layer with any other material. As indicated above, Ho does not teach a bond pad comprising a single layer comprised of only one type of metal and does not share the layer with any other material. Instead, Ho teaches a metal layer that DOES share the same layer with another type of material. Applicants again refer the Examiner to the copy of FIG. 6 of Ho which is included herewith as a mark-up, which indicates that FIG. 6 shows at least two different types of materials located on the same single layer. Simply put, neither Ho nor APA teach a single layer composed. Thus, because neither Ho nor the APA teach a wiring bond pad comprising a single metal layer, wherein the single metal layer does not share the single metal layer with any other material.

Additionally, Applicants point out to the Examiner that layer 52 of Ho is NOT an aluminum buffer layer. Applicants refer the Examiner to col. 4, line 30, in which layer 52 is referred to as a "gold capping layer 52," which is used to improve

adhesion between the bond pad 30 and gold wire 60. The term "capping" is not the same as "buffer". A buffer layer serves a different purpose, that is, as a "buffer" region, rather than a "capping" region. Layer 52 of Ho is also made from gold rather than aluminum. Thus, Ho does not teach aluminum buffer layer as taught by Applicants' invention. Based on the foregoing, the Applicants therefore submit that the rejection to claims 33-37 under 35 U.S.C. 103 (a) have been traversed. Applicants therefore request withdrawal of the rejection to claims 33-37 under 35 U.S.C. 103 (a).

Regarding claims 38-39, the Examiner argued that the combination of APA and Ho disclose all of the limitations of claims 38-39. The Applicants respectfully disagree with this assessment, submit that the arguments presented above with respect to the rejections to claims 29-37 apply equally to the rejection to claims 38-39. As indicated above, neither Ho nor APA, alone or in combination with one another teach a wiring bond pad formed from a single metal layer which does not share the same layer with any other material. Based on the foregoing, the Applicants therefore submit that the rejection to claims 38-39 under 35 U.S.C. 103 (a) have been traversed. Applicants therefore request withdrawal of the rejection to claims 38-39 under 35 U.S.C. 103 (a).

The Applicants also remind the Examiner that the Ho reference was issued on July 9, 2002, while Applicants' patent application was filed on January 9, 2002. Thus, because the Ho reference issued after Applicants' invention was filed, it is not clear that the Ho reference constitutes prior art for purposes of a rejection under 35 U.S.C. 103(a). In such a case, the Ho reference cannot properly combined with another reference such as APA as a basis for a rejection to claims 29-39 under 35 U.S.C. 103(a).

Additionally, the Examiner has not provided a motivation for combining Ho with APA as a basis for rejecting Applicants' claims 29-39. Why would one skilled in

the art have been motivated to combine two references that each does not teach a single metal layer that does not share the same layer with another material? Additionally, why would one skilled in the art have been motivated to have combined a reference (Ho), which did not even issue until after the Applicants' invention was filed. Such a motivation must be provided in order to assert a rejection under 35 U.S.C. 103(a).

The Applicants remind the Examiner that the language of the references may not taken out of context and combined them without motivation, in effect producing the words of the claims (and sometimes, not even the words or concepts of the claims), without their meaning or context. The resultant combination would not yield the invention as claimed. The claims are rejected under 35 U.S.C. §103(a) and no showing has been made to provide the motivation as to why one of skill in the art would be motivated to make such a combination, and further fails to provide the teachings necessary to fill the gaps in these references in order to yield the invention as claimed.

The rejections under 35 U.S.C. §103(a) have provided no more motivation than to simply point out the individual words of the Applicant's claims among the references, but without the reason and result as provided in the Applicant's claims and specification, and without reason as to why and how the references could provide the Applicant's invention as claimed. Hindsight cannot be the basis for motivation, which is not sufficient to meet the burden of sustaining a 35 U.S.C. §103(a) rejection.

Thus, claims 29-39 of the present invention are not taught or suggested by Ho and/or APA. Combining these references fails to teach or yield the invention as claimed. The combination of these references fails to teach or suggest all the elements of the claims. Further, one of skill in the art would not be motivated to make such a combination. Therefore, the present invention is not obvious in light

of any combination of Ho and/or APA. Withdrawal of the §103(a) rejection is therefore respectfully requested.

II. Conclusion

In view of the foregoing discussion, Applicants have responded to each and every rejection of the Official Action, and respectfully request that a timely Notice of Allowance be issued. Applicants have clarified the structural distinctions of the present invention and have amended the claims accordingly. Applicants believe that support for such amendments are provided by the Specification. Applicants respectfully submit that the foregoing discussion does not present new issues for consideration and that no new search is necessitated. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. 103(a), and further examination of the present application.

Should there be any outstanding matters that need to be resolved in the present application; the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

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